

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
an active area of a MOSFET separated by an element
isolation area on a semiconductor substrate;
5 at least one gate electrode provided to pass over
the active area; and
at least one source/drain contact formed on a
surface of the active area at one side of the gate
electrode,
10 wherein the gate electrode has a shape to vary so
that a gate length decreases with increasing a distance
from a position of the source/drain contact along the
gate electrode.
2. The semiconductor device according to claim 1,
15 wherein one gate electrode is provided in the active
area, and source/drain contacts are arranged at
respective sides of the gate electrode at diagonal
positions in the active area.
3. The semiconductor device according to claim 2,
20 wherein the MOSFET is one of a PMOSFET and an NMOSFET
of a CMOS inverter.
4. The semiconductor device according to claim 1,
wherein one gate electrode is provided in the active
area, and source/drain contacts are arranged at one end
25 of the gate electrode in a channel width direction.
5. The semiconductor device according to claim 1,
wherein the gate electrode has a planar pattern such

that the gate length varies in a laterally symmetrical form.

6. The semiconductor device according to claim 1, wherein the gate electrode has a planar pattern such
5 that the gate length varies in a laterally asymmetrical form.

7. The semiconductor device according to claim 1, wherein a silicide layer is formed on the surface of the active area at the opposite sides of the gate
10 electrode, and the source/drain contact is in contact with the silicide layer.

8. A semiconductor device comprising:
an active area separated by an isolation area on a semiconductor substrate and in which a plurality of
15 MOSFETS are arranged so as to be connected in series in the active area;

a plurality of gate electrodes juxtaposed with each other so as to pass over the active area;

20 a first source/drain contact formed at a side of the juxtaposed gate electrodes and in contact with a surface of the active area, and

a second source/drain contact formed at another side of the juxtaposed gate electrodes and in contact with a surface of the active area,

25 wherein the shape of the gate electrode located closest to one of the first and second source/drain contacts is formed to vary step by step or continuously

so that a gate length decreases with increasing a distance from a position of one of the first and second source/drain contacts along the gate electrode.

9. A semiconductor device according to claim 8,
5 further comprising at least one intermediate source/drain contact formed in contact with a source/drain area of an intermediate MOSFET corresponding to an intermediate one of the plurality of gate electrodes, and

10 wherein the gate electrode located closest to the intermediate source/drain contact has a shape formed to vary step by step or continuously so that the gate length decreases with increasing distance from the position of the intermediate source/drain contact along
15 the gate electrode.

10. The semiconductor device according to claim 8,
wherein the plurality of MOSFETS form a NAND type memory unit in a NAND type flash memory.

11. The semiconductor device according to claim 8,
20 wherein the first and second source/drain contacts arranged at the respective sides of the gate electrode are arranged at diagonal positions in the active area.

12. The semiconductor device according to claim 8,
wherein the first and second source/drain contacts
25 arranged at the respective sides of the gate electrode are arranged at the same end of the gate electrode in a channel width direction.

13. The semiconductor device according to claim 8,
wherein the gate electrode has a planar pattern such
that the gate length varies in a laterally symmetrical
form.

5 14. The semiconductor device according to claim 8,
wherein the gate electrode has a planar pattern such
that the gate length varies in a laterally asymmetrical
form.